REMARKS

Claims 21-29 are pending in this application. Claims 1-20 have been cancelled without prejudice to the subject matter.

Specification

The office action objects to the specification for using the term "nwell" rather than "n-well" or "n well" to refer to, e.g., nwell 113. Applicants respectfully traverse the objection.

Applicants believe the term "nwell" is commonly used in the industry and is used interchangeably with the other suggested terms. For example, the 1999 IEDM publication "100nm Gate Length High Performance Low Power CMOS Transistor Structure" by T. Ghani et al., of Intel Corporation (a copy of selected pages are attached to this amendment, and the full document can be found at *www.intel.com/research/silicon/100nmidem99p.pdf*) uses the term "nwell". Therefore, no confusion will result from the use of the term "nwell". In addition, it is well established that the applicants can be their own lexicographers so long as the terms used are not repugnant to their ordinary meaning. MPEP §706.03(d), (citing *In re Hill*, 161 F.2d 367, 73 U.S.P.Q. 482 (CCPA 1947)). Given the lack of standardization of the spelling of the term and the several variations in common use, applicants believe the version used in the specification and abstract is appropriate and not repugnant to its ordinary meaning.

Thus, Applicant respectfully believes the objection to have been overcome.

Rejections under 35 U.S.C. §112

Claims 8 and 9 are rejected under 35 U.S.C. §112(2p). Claims 8 and 9 have been cancelled rendering moot the rejection with respect to those claims.

Therefore, Applicant respectfully believes the rejection under 35 U.S.C. § 112 is overcome.

Rejections under 35 U.S.C. §102

Kikuchi

Claims 1, 4, 5, 7, 10, 11, 14-16 and 19 are rejected under 35 U.S.C. §102(e) as being unpatentable over Kikuchi et al. (U.S. Patent Application Publication 20010036694A1). Claims 1-20 have been cancelled rendering the rejection moot. New claims 21-29 have been added.

New claim 21 recites among other things, a method of making a semiconductor device (e.g., 100) comprising, among other things, growing an oxide (e.g., 103) less than one thousand angstroms thick over a drain (e.g., 110) of a first conductivity type, and introducing dopants of a second conductivity type through the oxide to form a first charge balancing layer (e.g., 108) within the drain and at a surface of a substrate.

The Kikuchi reference discloses in FIG. 3 a method of making a p-channel high voltage MOS device on a P-type substrate 12 having an N-type well region 2. P-type impurities are implanted into a drain extension LP layer 4 to form a drain contact 12. P-type FP layers 7A are formed

within drain extension LP layer 4. Hence, substrate 12, drain extension LP layer 4, drain contact 12 and FP layers 7A are all P-type, i.e., a first conductivity type, while well region 2 is N-type, i.e., a second conductivity type.

The Kikuchi reference does not disclose forming a drain of a first conductivity type and introducing dopants of a second conductivity type through an oxide to form a charge balancing layer within the drain. All of the Kikuchi doped regions are P-type except for nwell 2. The reference does not disclose a charge balancing layer, or a charge balancing layer formed by implanting dopants through an oxide, or a charge balancing layer formed within a drain, or a charge balancing layer having the opposite conductivity type as the drain. Consequently, the reference device does not have the advantage of producing more predictable charge balancing layer.

Thus, a rejection of new claim 21 in view of the Kikuchi reference is respectfully believed to have been overcome, and should be allowable. Since new claims 22-29 depend from new claim 21, they should be allowable for at least the same reasons.

Sogo

Claims 1, 4, 5, 8-11, 13, 15 and 16 are rejected under 35 U.S.C. §102(e) as being unpatentable over Sogo (U.S. Patent 6,312,996). Claims 1-20 have been cancelled rendering the rejection moot. New claims 21-29 have been added.

New claim 21 recites among other things, a method of making a semiconductor device (e.g., 100) comprising

providing a substrate (e.g., 101) having a surface for forming a channel (e.g., 115), forming a drain (e.g., 106, 110) of a first conductivity type at the surface, growing an oxide (e.g., 103) less than one thousand angstroms thick over the drain, and introducing dopants of a second conductivity type through the oxide to form a first charge balancing layer (e.g., 108) within the drain and at the surface.

The Sogo reference discloses in FIG. 8C a method of making a semiconductor device comprising growing a one micron thick field oxide 34 on the top of drain 33 and then implanting a buried region 37 within the drain as described in column 13 line 30 through column 14 line 10 of the reference.

The Sogo reference does not show or teach implanting through an oxide less than one thousand angstroms thick to form a charge balancing layer at the surface and within a drain as does the applicant. The Sogo reference instead shows and teaches implanting through a one micron thick field oxide 34 to form a buried region 37 inside the extended drain region 33 (c13, lines 35-45 and c14, lines 5-10).

Thus, as Sogo is forming the buried region 37 away from the surface, rather than at the surface as does the applicant, the reference device does not have the advantage of having a higher breakdown voltage resulting from the concentration of dopants at the surface of the nwell region being greater than a device having a buried region 37 within the extended drain.

Thus, a rejection of new claim 21 in view of the Sogo reference is respectfully believed to have been overcome, and should be allowable. Since new claims 22-29 depend from new claim 21, they should be allowable for at least the same reasons.

Nishibe et al.

Claims 1-3, 11-12, 15, 18 and 20 are rejected under 35 U.S.C. §102(e) as being unpatentable over Nishibe et al. (U.S. Patent 6,399,468 B2). Claims 1-20 have been cancelled rendering the rejection moot. New claims 21-29 have been added.

New claim 21 recites among other things, a method of making a semiconductor device (e.g., 100) comprising, among other steps, forming a drain (e.g., 106, 110, 113) of a first conductivity type (e.g., n-type), growing an oxide (e.g., 103) less than one thousand angstroms thick over the drain, and introducing dopants of a second conductivity type (e.g. p-type) through the oxide between the channel and a drain contact (e.g., 106) to form a first charge balancing layer (e.g., 108) within the drain.

The Nishibe et al. reference discloses in FIG.'s 3-6 a method of making a semiconductor device comprising implanting p-type substrate 101 with n-type dopants to form an n-type middle layer or SLN layer 106 in an n-type extended drain region 103 between channel 112 and an n-type drain electrode 116 as described in column 5 though 6 of the reference. The Nishibe et al. reference also discloses SLN layer 106 formed having drain diffusion 111 contained within.

The Nishibe et al. reference does not disclose introducing dopants of a second conductivity type (e.g., p-type) through an oxide between a channel and a drain contact to form a first charge balancing layer within a drain of a first conductivity type as does the applicant. The Nishibe et al. reference has the middle layer or SLN layer 106 formed between the drain contact and the channel, but layer 106 is the same conductivity type (n-type) as the drain, not opposite as claimed.

Thus, a rejection of new claim 21 in view of the Nishibe et al. reference is respectfully believed to have been overcome, and should be allowable. Since new claims 22-29 depend from new claim 21, they should be allowable for at least the same reasons.

Kobyashi

Claims 1, 4, 6 and 15-17 are rejected under 35 U.S.C. §102(e) as being unpatentable over Kobayashi (U.S. Patent 6,346,448). Claims 1-20 have been cancelled rendering the rejection moot. New claims 21-29 have been added.

New claim 21 recites among other things, a method of making a semiconductor device (e.g., 100) comprising, among other things, forming a drain (e.g., 106, 110, 113) of a first conductivity type (e.g., n-type) and introducing dopants of a second conductivity type (e.g. p-type) through an oxide to form a first charge balancing layer (e.g., 108) within the drain.

The Kobayashi reference discloses in FIG.'s 7A-7B a method of making a DRAM comprising implanting p type substrate PSUB with p type dopants to form the region PWELL

in n type well region NWELL, and then forms a lightly doped drain (LDD) regions within PWELL.

The Kobayashi reference does not disclose introducing dopants of a second conductivity type (e.g., p-type) through the oxide to form a first charge balancing layer within a drain of a first conductivity type as claimed.

Thus, a rejection of new claim 21 in view of the Kobayashi reference is respectfully believed to have been overcome, and should be allowable. Since new claims 22-29 depend from new claim 21, they should be allowable for at least the same reasons.

Therefore, Applicant respectfully believes the rejection under 35 U.S.C. § 102 is overcome.

Applicant has reviewed the other prior art made of record and believes that such art does not affect the patentability of the invention as claimed.

Conclusion

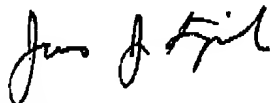
Applicants respectfully request entry of this amendment and early and favorable acceptance of this application.

A two month extension fee of $410.00 is believed due by filing this Amendment. However, the Commissioner is hereby authorized to charge any fees due or credit any overpayment to Deposit Account 501086.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,

Mohamed Imam et al.



James J. Stipanuk
Attorney for Applicant(s)
Reg. No. 44,358
Tel. (602) 244-4885

ON Semiconductor
Law Dept./MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

Date: 12-5-2002

100 nm Gate Length High Performance Low Power CMOS Transistor Structure

T. Ghani, S. Ahmed, P. Aminzadeh, J. Bielefeld, P. Charvat, C. Chu, M. Harper, P. Jacob, C. Jan, J. Kavalieros, C.Kenyon, R. Nagisetty, P. Packan#, J. Sebastian, M.Taylor, J. Tsai, S. Tyagi, S. Yang , M. Bohr*

Portland Technology Development, *QRE, #TCAD

Intel Corporation

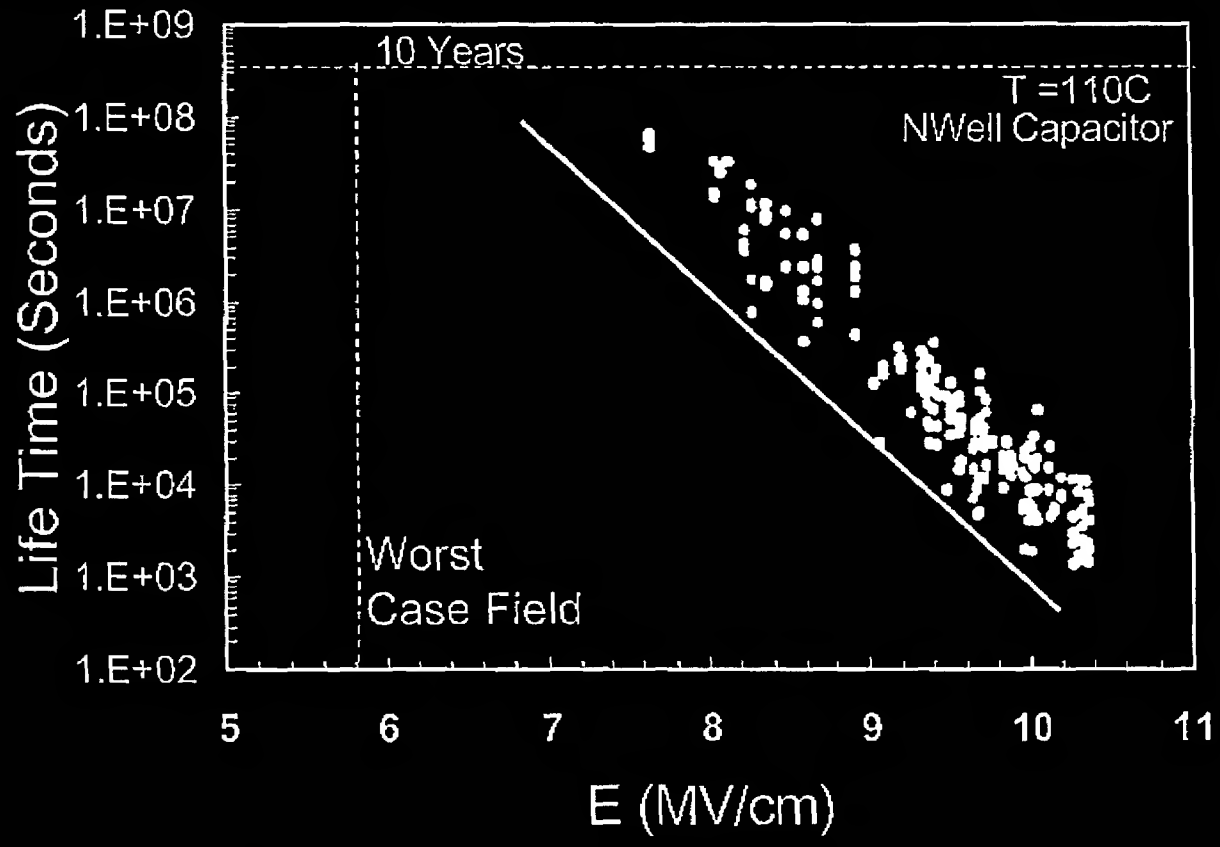
1999 IEDM

intel

Area Junction Capacitance

- Very low C_{JA} achieved without compromising isolation - int

2nm Physical Gate Oxide Lifetime



- Some data points correspond to 1.5 years stress
- Product V_{CC} is set based on oxide area and temperature
- Gate oxide meets 10 years life time criteria